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Design and Implementation of DSP based High Frequency Three Phase SPWM Generator

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***Abstract*—Nowadays power electronic DC/AC inverters are widely used in energy conversion and motor control application. Higher-frequency SPWM (Sinusoidal Pulse Width Modulation) waves can decrease the size of passive component in the inverter, achieving a low volume and a lightweight as needed. This paper presents a DSP based SPWM generator, which can operate at switching frequencies up to 1 MHz, thus it can meet the high switching frequency demands of modern DC/AC inverters. The proposed design is based on the MCPWM (Motor Control Pulse Width Modulation) block which is available in the DSPIC, and it is verified using the DsPIC30F2010 controller and a test setup to filter the PWM. The experimental results confirm that this SPWM generator achieves much faster switching frequency, less harmonic interference, and higher resolution of SPWM waveforms, showing a better performance compared to past design.**

***Index Terms*— Digital Signal Processor (DSP); high frequency; inverter; SPWM generator.**

I. INTRODUCTION

With the dc/ac inverters widely applied in renewable energy grid system, frequency converter, uninterruptible power supply (UPS), research on high-frequency Pulse width modulation (PWM) inverter is gaining more and more attention [1]. The PWM technique is used for inverters with an appropriate switching scheme to produce a desired AC output fed from DC input. And the SPWM switching technique, using a standard sinusoidal waveform as PWM modulation wave, is one of the most popular inverter control methods.

Nowadays, power converters are evolving toward designs with higher switching frequencies in order to reduce the size of inductors and capacitors [2]. The dc/ac inverter typically operates at switching frequencies ranging from 1 kHz to 100 kHz [3, 4]. But recent developments in semiconductor technology enable the use of higher switching frequencies through SiC [5] and GaN [6] power devices, which feature faster switching speeds with reasonably low losses. This allows the design of power dc/ac inverters with reduced size and cost, and improved dynamic behavior and power density. Typically, microprocessors, DSPs or Field Programmable Gate Arrays (FPGAs) are used for the implementation of SPWM generator. Microprocessor-based digital controls schemes have been applied to the PWM inverters for sinusoidal waveform synthesis

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[7]. However, due to the high switching frequency required, it may limit the functionality of the microprocessor to perform various tasks.
Several FPGA-based solutions have been proposed in the literature [1, 8-9]. One common solution is to use an up-down counter to form the triangular wave. The corresponding samples of modulation and carrier waves are stored in digital format in a lookup table (LUT) implemented in the FPGA internal memory. In [8], a third-order 100-kHz SPWM wave is produced based on the Altera Cyclone II series FPGA. In [1] and [9], the values of both the reference sine and triangular waves are stored in the FPGA device Block RAMs (BRAMs) in order to exploit their one-clock-cycle access time. This architectural allows the SPWM generator operates at the switching frequencies up to 1MHz.
Using DSPs for the design of the dc/ac inverters has always been the first choice for Engineers. Compared to the FPGA based circuit, DSPs can't only provide the high-frequency SPWM generator, but also offer A/D, D/A channels and specialized algorithm libraries, thus simplifying the design of control circuit and reduce the cost. This paper presents a DSP based SPWM generator, which can also operate at 1 MHz switching frequencies. We use the DSPIC including MCPWM peripherals.
The MCPWM on DsPIC microcontroller enables to generate and run three independent PWM with high resolution and center aligned PWM which provides timing accuracy in the generated PWM. MCPWM also provides a PWM interrupt generation option which makes it convenient to update the sine PWM at the required PWM rate.
The principle for generating three independent PWM is explained in section II. The corresponding configuration and calculation of MCPWM module is analyzed in Section III, and the experimental results of the proposed architecture and inverter prototype are shown in Section IV. Finally the conclusions of this study are drawn in Section V.

II. DESIGN OF THE PROPOSED SPWM GENERATOR

A. SPWM Technique Overview

SPWM is a technology of inverter-controlled which uses the desired sine wave as modulation waveform and uses triangle (or saw tooth) wave whose frequency is much higher than the modulation wave as the carrier waveform [2].

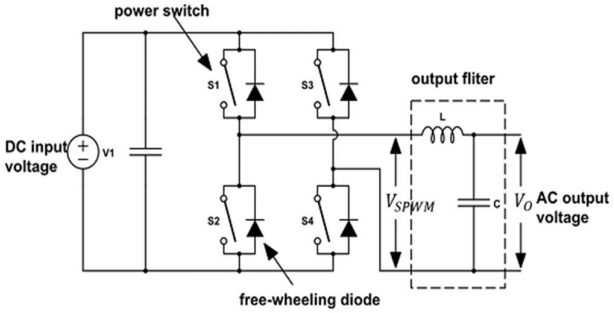

Fig 1. Block diagram of single phase, full-bridge inverter.

Fig. 1 shows a simplified block diagram of a single phase, full-bridge inverter. The on and off states of power switches S1, S2, S3, S4, (e.g. MOS, IGBTs, etc.) will be generated when the instantaneous value of the reference signal is larger than the triangular carrier (Fig. 2). After generated unipolar SPWM pulses, *U*SPWM, filtered by the low-pass LC type filter, then we can get the desired AC output. In engineer we often use average-value model to simplify the calculation of the voltage of output fundamental wave, and the amplitude is calculated as follows:

$$V_o = M_a \cdot V_d = \frac{V_r}{V_c} \cdot V_d \qquad (1)$$

Where *V*d(V) is the DC input voltage, *V*r(V) and *V*c(V) are the sine modulation wave and carrier amplitudes, respectively, and is amplitude modulation index.

In digital control, regular sampling method is often used to generate SPWM waves. The sine modulation wave is sampled with a sampling frequency equal to. Due to the limited storage capacity in the DPSs, it's hard to store all the sine wave sample values of every switching period. As the regular-sampled PWM technique explained in [11], we can calculate the pulse width once and use it over *N* consecutive switching periods of the SPWM wave. Then the switching frequency is *N* times that of the new sampling sine wave, that is:

$$f_s = \frac{f_c}{N} \qquad (2)$$

In result, the size of the table storing the digital sample values and calculation numbers are also *N* times less than the past one.

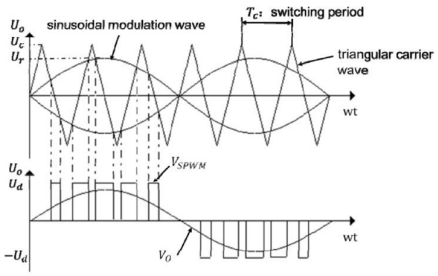

Fig. 2. Waveform of the SPWM inverter circuit.

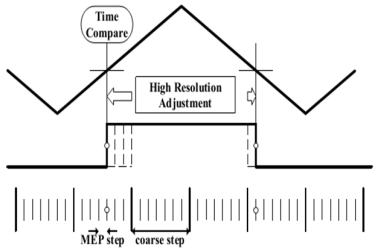

Fig 3. Operating logic of PWM Module.

B. Algorithm for Generation of phase shifted signals.

Generation of single phase signal is as simple that the duty cycle value of sine table is updated every PWM Period. But the generation of 3 Phase needs a special algorithm to generate and maintain the 120 degree phase shift between each generated phases of the SPWM. On the other hand generation of three phases SPWM using independent sine wave LUT guarantees only synchronization with respect to itself not between each phases of the 3 PWMs. So a special methodology of Direct Digital Synthesis is implemented to guarantee a phase synchronized and phase corrected signals. The methodology of generation is briefly explained in the below section.

Here's a breakdown of the internal circuitry of a DDS device: its main components are a phase accumulator, a means of phase-to-amplitude conversion (often a sine look-up table), and a DAC. These blocks are represented in Figure 4. A DDS produces a sine wave at a given frequency. The Frequency depends on two variables, the reference-clock frequency and the binary number programmed into the frequency register (tuning word). The binary number in the frequency register provides the main input to the phase accumulator. If a sine look-up table is used, the phase accumulator computes a phase (angle) address for the look-up table, which outputs the digital value of amplitude - corresponding to the sine of that phase angle to the DAC. The DAC, in turn, converts that number to a corresponding value of analog voltage or current. To generate a fixed-frequency sine wave, a constant value (the phase increment—which is determined by the binary number) is added to the phase accumulator with each clock cycle. If the phase increment is large, the phase accumulator will step quickly through the sine look-up table and thus generate a high frequency sine wave. If the phase increment is small, the phase accumulator will take many more steps, accordingly generating a slower waveform.

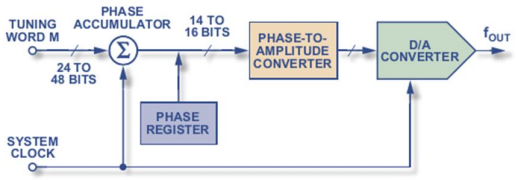

Fig 4. Conceptual diagram of DDS.

$$\text{fout} = \frac{M * fc}{2^n} \qquad (3)$$

The phase accumulator is actually a modulo –M counter that increments its stored number each time it receives a clock pulse. The magnitude of the increment is determined by the binary-coded input word (M). This word forms the phase step size between reference - clock updates; it effectively sets how many points to skip around the phase wheel. The larger the jump size, the faster the phase accumulator overflows and completes it equivalent of a sine -wave cycle. The number of discrete phase points contained in the wheel is determined by the resolution of the phase accumulator (n), which determines the tuning resolution of the DDS. For an n= 28 -bit phase accumulator, an M value of 0000...0001 would result in the phase accumulator overflowing after 228 reference - clock cycles (increments). If the M value is changed to 0111...1111, the phase accumulator will overflow after only 2 reference - clock cycles (the minimum required by Nyquist).The equation 3 shows the relation between output frequency and M count values.

III. WORKING PRINCIPLE

Schematic diagram of three phase inverter is shown in figure5. DC supply used as an input of three phase inverter. Three phase inverter block consist a hex bridge with LC filter circuit. The ac output of inverter is given to the load. In control circuit dsPIC is used for SPWM gate pulse generation.

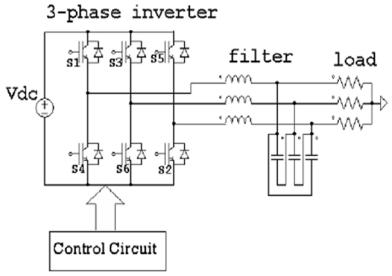

Fig 5. 3 phase inverter schematic

Figure 6 shows the required SPWM pulse pattern for three phase inverter. The reference waveform is the desired output waveform [5]. Whenever the voltage level of the sinusoidal waveform is higher than the triangular waveform, a logic '1' signal is generated. Otherwise, it is logic '0'. As a result, the controller produces SPWM gating signals to turn the switching devices on and off accordingly. Consequently, the inverter produces output voltage waveform resemble to the SPWM waveform. Then, the output voltages pass through the filter to removes higher harmonics from the waveform and make the waveform nearly sinusoidal.

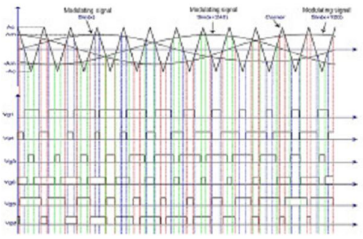

Fig 6. Switching scheme for 3 phase inverter

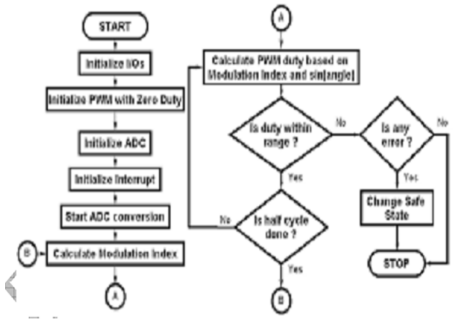

Fig 6A. Flow chart for SPWM Technique

If we observe first 100 pulses which are held between 0 to 90 degree angles of reference wave, the duty cycle is increases. In same manner from 90 to 180 degree, it is decreasing. From 180 to 270, next 100 pulses are in form of decrementing. Once again they are in incrementing form in 270 to 360 degree. This cycle is repeated at 120 degree apart for second phase and for third phase it is situated at 240 degree. As we change the modulation index, the pulse width is changed.

Fig 6A shows the flowchart for SPWM generation. The duty cycle is updated on every interrupt generated by the PWM Module. PWM module is configured to work at 200KHz. Every 4 PWM interrupts the output is read using ADC to adjust the Modulation Index of the PWM. Three independent PWMs are updated using 3

ADCs available on dsPIC and the 3 Indices are adjusted according to their corresponding ADC channels. The output are filtered using a simple RC filter for demonstration purpose

IV. RESULTS

The above figure shows the hardware test setup built to test the design. The design is successfully implemented on a dsPIC. The hardware setup consists of a simple RC filter to filter out the High frequency SPWM signal.

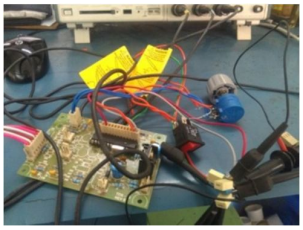

Fig 7A: Hardware setup of the design

Fig 7B: Output waveform

Figure 7B shows the resultant waveform of the design. We can observe the phase shifted waveforms in the figure.

V. CONCLUSION

The 3 phase SPWM with DDS logic is successfully implemented in hardware and the idea is executed successfully. Various logics like compliment pulse, dead band, varying duty cycle can be implemented in dsPIC controller by setting of proper available registers. Nearer to 30 MIPS speed of controller is obtained by the given PLL logic. All six pulses of 5volts are obtained. By applying the same logic hardware is also developed. Modulation logic is also checked from range of 0 to 5 volts for 0 to 0.96 modulation index with ADC interfacing. Close loop controlling can be added in future for complete implementation.

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